Amendments to the Drawings

Submitted herewith are two (2) sheets of Replacement drawings with Figures 1 and 2, corresponding to the above-captioned application. The two (2) sheets of Replacement drawings are to replace Figures 1 and 2 as filed on May 21, 2007. Identification of the drawings is provided in accordance with 37 C.F.R. § 1.84(c). Acknowledgment of the receipt, approval, and entry of these drawings into this application is respectfully requested.

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 8 and 10-13 are pending in the application, with claim 8 being the sole independent claim. Claims 8 and 10-13 are sought to be amended. Claim 9 is sought to be cancelled without prejudice to or disclaimer of the subject matter therein. Applicants submit herewith Replacement drawings to replace the drawings filed on May 21, 2007. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Objections to the Drawings

The Examiner has objected to the drawings because of numerous alleged informalities. Without acquiescing to the merits of this allegation, Applicants have submitted herewith replacement drawings for FIG. 1 and FIG. 2. Applicants note that the multiplexer depicted in FIG. 1 and FIG. 2 is a conventional 2-to-1 multiplexer. It is well known that a schematic symbol for a multiplexer is an isosceles trapezoid with a longer parallel side containing input data and a shorter parallel side containing output data. A select line, to connect a desired input to the output, is located on a top side of the isosceles trapezoid. Descriptions for these conventional features have been omitted from the instant application. (*see*, MPEP § 2164.01). Further, FIG. 1 illustrates a conventional counter and FIG. 2 illustrates a counter including the jitter elements according to an embodiment of the present invention. It is well known that counters include a data input

containing digital information along with a latch input to hold the data in the counter. Applicants respectfully request the acknowledgment of the receipt, approval, and entry of these drawings into this application. Accordingly, Applicants respectfully request the objection to the drawings be withdrawn.

Objections to the Specification

The Examiner has objected to the specification because of numerous alleged informalities. Without acquiescing to the merits of this allegation, Applicants have amended the specification to accommodate the Examiner's rejection. Accordingly, Applicants respectfully request the objection to the specification be reconsidered and withdrawn.

Rejections Under 35 U.S.C. § 112

Claim 9 stands rejected under 35 U.S.C. § 112, first paragraph, for allegedly failing to comply with the enablement requirement. Without acquiescing to the merits of this allegation, Applicants have cancelled claim 9 rendering the rejection under 35 U.S.C. § 112, first paragraph, moot.

Rejections Under 35 U.S.C. § 102

Benis

Claims 8, 9, and 11-13 stand rejected under 35 U.S.C. § 102(a) as allegedly being anticipated by United States Patent Application Publication No. 2003/0125916 to Benis (herein "Benis"). Applicants respectfully traverse the rejection and provide the following arguments to support patentability.

Applicants respectfully submit that the claim 8 as amended is patentable over the art of record. For example, Benis does not teach nor suggest at least the features of "a first and a second asynchronous clock domain, wherein jitter elements are additionally insertable in the second asynchronous clock domain at predetermined portions of circuit boundaries between the first and the second asynchronous clock domain, the jitter elements being representable as logical elements, the values of which are randomly set, wherein at least one of the jitter elements is configured to jitter data from the first asynchronous clock domain," as recited by claim 8.

Benis discloses a "method for simulating and synthesizing an array of flip-flops, including metastable effects." (*see*, Benis, para. [0001]). To "simulate the array of flip flops and in particular to model metastable effects, three registers 480, 482 and 484 are defined for simulation of the circuit only (that is, these registers are not used for synthesis of the circuit)." (*see*, Benis, para. [0035]). Benis further provides that

> the simulation of the array with metastable effects also includes a simulated multiplexer (MUX) 460 that receives inputs from registers 480 and 482, multiplexes those inputs, and provides outputs to register 484. In this embodiment, MUX 460 multiplexes the inputs from registers 480 and 482 responsive to [a random number generator 470].
>
> (*see*, Benis, para. [0036]).

Assuming *arguendo* that the three registers 480, 482, and 484, the simulated multiplexer 460, and the random number generator 470 comprise "jitter elements," Benis does not teach or suggest at least the "jitter elements [that] are additionally insertable in the second asynchronous clock domain at predetermined portions of circuit boundaries between the first and the second asynchronous clock domain" as recited by claim 8. Benis is silent regarding the location of the three registers 480, 482, and 484, the simulated multiplexer 460, and the random number generator 470 relative to the asynchronous clock domains.

In fact, FIG. 4A of Benis suggests that these elements are located external to or outside of the first and the second asynchronous clock domains. Thus, Benis does not teach nor suggest at least the features of "a first and a second asynchronous clock domain, wherein jitter elements are additionally *insertable in the second asynchronous clock domain* at predetermined portions of circuit boundaries between the first and the second asynchronous clock domain, the jitter elements being representable as logical elements, the values of which are randomly set, wherein at least one of the jitter elements is configured to jitter data from the first asynchronous clock domain." (*emphasis added*, *see*, claim 8, as amended)

For the reasons discussed above, Benis does not teach each and every feature of claim 8. Consequently, Benis cannot anticipate claim 8. Applicants have cancelled claim 9 rendering this rejection under 35 U.S.C. § 102(a) moot. Dependent claims 11-13 are likewise not anticipated by Benis for the same reasons as discussed above and further in view of their own respective features. Accordingly, Applicants respectfully requests that the rejection of claims 8 and 11-13 under 35 U.S.C. § 102(a) be reconsidered and withdrawn.

Sharma

Claims 8-10, 12, and 13 stand rejected under 35 U.S.C. § 102(a) as allegedly being anticipated by United States Patent No. 6,598,191 to Sharma et al. (herein "Sharma"). Applicants respectfully traverse the rejection and provide the following arguments to support patentability.

Applicants respectfully submit that the claim 8 as amended is patentable over the art of record. For example, Sharma does not teach nor suggest at least the features of "a

first and a second asynchronous clock domain, wherein jitter elements are additionally insertable in the second asynchronous clock domain at predetermined portions of circuit boundaries between the first and the second asynchronous clock domain, the jitter elements being representable as logical elements, the values of which are randomly set, wherein at least one of the jitter elements is configured to jitter data from the first asynchronous clock domain" as recited by claim 8.

Sharma discloses an apparatus "for verifying the asynchronous boundary behavior of a digital system...where the asynchronous boundary is formed between two or more clock domains in the digital system." (*see*, Sharma, col. 1, lines 6-10). One embodiment of Sharma "illustrates in schematic block diagram from a [model] having a separately clocked write [domain] and a separately clock read [domain], adjacent [the write domain], wherein additional logic has been inserted in [the write domain] to allow proper verification of the asynchronous boundary behavior between the domains." (*see*, Sharma, col. 7, lines 51-55; *see also*, Sharma, col. 7, line 51 through col. 9, line 67 and FIG. 4). In other words, this embodiment of Sharma inserts additional logic in the write domain, i.e., the first asynchronous clock domain. Clearly, this embodiment of Sharma does not teach or suggest "a first and a second asynchronous clock domain, wherein jitter elements are additionally *insertable in the second asynchronous clock domain* at predetermined portions of circuit boundaries between the first and the second asynchronous clock domain, the jitter elements being representable as logical elements, the values of which are randomly set, wherein at least one of the jitter elements is configured to jitter data from the first asynchronous clock domain." (*emphasis added*, *see*, claim 8, as amended).

Another embodiment of Sharma "illustrates in schematic block diagram from a [model] having a separately clocked write [domain] and a separately clocked read

[domain], wherein additional logic has been inserted in [the read domain] to allow proper verification of the asynchronous boundary behavior between the domains." (*see*, Sharma, col. 11, lines 44-54; *see also*, Sharma, col. 11, line 44 through col. 13, line 5 and FIG. 7). This embodiment inserts extend flip flops and multiplexers in the read domain rather than the write domain. Outputs of first level read flip flops are coupled to inputs of the extend flip flops. The outputs of first level read flip flops are also coupled to inputs of the multiplexers. (*see*, Sharma, col. 11, line 55 through col. 12, line 57). Each multiplexer output is connected to a corresponding input of a second level read flip flop. (*see*, Sharma, col. 11, line 55 through col. 12, line 57). In other words, assuming *arguendo* that the extend flip flops and the multiplexers comprise "jitter elements," these elements of Sharma do not jitter data from the write domain, i.e., the first asynchronous clock domain, rather these elements jitter data from the first level read flip flops that are located in the read domain, i.e., the second asynchronous clock domain. Clearly, this embodiment of Sharma does not teach or suggest "a first and a second asynchronous clock domain, wherein jitter elements are additionally insertable in the second asynchronous clock domain at predetermined portions of circuit boundaries between the first and the second asynchronous clock domain, the jitter elements being representable as logical elements, the values of which are randomly set, wherein *at least one of the jitter elements is configured to jitter data from the first asynchronous clock domain*." (*emphasis added*, *see*, claim 8, as amended).

For reasons discussed above, Sharma does not teach each and every feature of claim 8. Consequently, Sharma cannot anticipate claim 8. Applicants have cancelled claim 9 rendering this rejection under 35 U.S.C. § 102(a) moot. Dependent claims 10, 12, and 13 are likewise not anticipated by Sharma for the same reasons as discussed above

and further in view of their own respective features. Accordingly, Applicants respectfully requests that the rejection of claims 8, 10, 12, and 13 under 35 U.S.C. § 102(a) be reconsidered and withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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Appendix A: Replacement Drawings